L5: Entry 3 of 43 File: USPT Jul 10, 2001

DOCUMENT-IDENTIFIER: US 6260088 B1
**** See image for Certificate of Correction ****
TITLE: Single integrated circuit embodying a risc processor and a digital signal processor

Detailed Description Text (7):
As shown in FIG. 1, there is a set of parallel processors 100-103 and a master processor 12 connected to a series of memories 10 via a cycle-rate local connection network switch matrix 20 called a crossbar switch. The crossbar switch, as will be shown, is operative on a cycle by cycle basis to interconnect the various processors with the various memories so that different combinations of distributed and shared memory arrangements can be achieved from time to time as necessary for the particular operation. Also, as will be shown, certain groups of processors can be operating in a distributed mode with respect to certain memories, while other processors concurrently can be operating in the shared mode with respect to each other and with respect to a particular memory.

Detailed Description Text (37):
Turning now to FIG. 15, the MIMD mode is shown such that processors 100-103 are connected through crossbar switch 20 to various memories. Typically, these connections would last through several cycles and thus, the processors each would be connected to the respective memories for a period of time. While this is not necessary, it would be the most typical operation in the MIMD mode. For any processor, or group of processors operating in the MIMD mode of FIG. 15, crossbar switch 20 can, on a cycle by cycle basis, be operated so that data from a particular memory element is immediately made available to any of the other processors so that the data can either be cycled through the other processors or operated on a one-time basis.

Detailed Description Text (44):
Transfer processor 11 shown in FIGS. 1 and 2 and in FIG. 57 transfers data between external memory and the various internal memory elements. Transfer processor 11 is designed to operate from packet requests such that any of the parallel processors or the master processor can ask transfer processor 11 to provide data for any particular pixel or a group of pixels or data, and the transfer processor will transfer the necessary data to or from external and internal memory without further processor intervention instructions. This then allows transfer processor 11 to work autonomously and to process data in and out of the system without monitoring by any of the processors. Transfer processor 11 is connected to all of the memories through switch matrix 20 and is arranged to contend with the various links for access to the memories. Transfer processor 11 for any particular link may be assigned the lowest priority and access a memory when another processor is not accessing that memory. The data that is being moved by the transfer processor is not only the data for processing pixels, but instruction streams for controlling the system. These instruction streams are loaded into the instruction memory via crossbar switch 20. Transfer processor 11 can be arranged with a combination of hardware and software to effect the purpose of data transfer.

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L5: Entry 3 of 43 File: USPT Jul 10, 2001

US-PAT-NO: 6260088
DOCUMENT-IDENTIFIER: US 6260088 B1
** See image for Certificate of Correction **

TITLE: Single integrated circuit embodying a risc processor and a digital signal processor

DATE-ISSUED: July 10, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Gove; Robert J.	Plano	TX		
Balmer; Keith	Bedford			GB
Ing-Simmons; Nicholas Kerin	Bedford			GB
Guttag; Karl Marion	Missouri City	TX		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Texas Instruments Incorporated	Dallas	TX			02

APPL-NO: 09/ 517990 [PALM]
DATE FILED: March 3, 2000

PARENT-CASE:
This application is a divisional of U.S. patent application Ser. No. 08/264,582 filed Jun. 22, 1994 now U.S. Pat. No. 6,070,003; which is a continuation of U.S. patent application Ser. No. 07/437,852 filed Nov. 17, 1989, now abandoned.

INT-CL: [07] G06 F 13/00

US-CL-ISSUED: 710/100; 710/131, 712/20, 712/35, 712/41
US-CL-CURRENT: 710/100; 712/20, 712/35, 712/41

FIELD-OF-SEARCH: 710/100, 710/101, 710/131, 710/132, 712/20, 712/21, 712/22, 712/10, 712/28, 712/34, 712/35, 712/41, 712/43

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4622632	November 1986	Tanimoto et al.	

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☐	5513346	April 1996	Satagopan et al.	714/48
☐	5890013	March 1999	Nair et al.	710/53

ART-UNIT: 215

PRIMARY-EXAMINER: Etienne; Ario

ATTY-AGENT-FIRM: Marshall, Jr.; Robert D. Brady, III; W. James Telecky, Jr.; Frederick J.

ABSTRACT:

A single integrated circuit includes first and second data processors operating on different instruction sets independently operating on disjoint programs and data. The single integrated circuit preferably includes an external interface, a shared data transfer controller and shared memory divided into plural independently accessible memory banks. The two data processors are preferably a digital signal processor (DSP) and a reduced instruction set computer (RISC) processor. The DSP and RISC processors are suitably programmed to perform differing aspects of computer image processing.

37 Claims, 64 Drawing figures

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L5: Entry 4 of 43 File: USPT Jun 12, 2001

DOCUMENT-IDENTIFIER: US 6246629 B1
TITLE: Semiconductor IC device having a memory and a logic circuit implemented with a single chip

Brief Summary Text (14):
On the other hand, the second prior art concerns a coupling circuit for coupling memories and processors. In this second prior art, data transfer paths between the individual memories and the processors can be changed over to each other in various ways by crossbar switches. According to the second prior art, however, since the crossbar switches are used, a subject based on the above-mentioned second subject is caused. Namely, the second prior art has a subject that as the number of coupling lines is increased, the number of switches becomes enormous with an increase in scale of hardware and also an increase in delay. In the case where the data transfer paths between plural memories and plural processors independent of each other are changed over, as in the second prior art, a system used in the conventional parallel computer can be realized on the same chip, as it is, since the number of memories and processors is generally small. However, in the case where the correspondence between a group of several-hundred or more I/O lines of a memory and a group of I/O lines of a logic circuit such as operation circuit is changed over, the requirements for the degree of integration and the operating speed are severe and it is therefore difficult to use the conventional system, as it is.

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L5: Entry 4 of 43 File: USPT Jun 12, 2001

US-PAT-NO: 6246629
DOCUMENT-IDENTIFIER: US 6246629 B1

TITLE: Semiconductor IC device having a memory and a logic circuit implemented with a single chip

DATE-ISSUED: June 12, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Watanabe; Takao	Fuchu			JP
Ayukawa; Kazushige	Kokubunji			JP
Fujita; Ryo	Hitachi			JP
Yanagisawa; Kazumasa	Kokubunji			JP
Tanaka; Hitoshi	Ome			JP

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Hitachi, Ltd.	Tokyo			JP	03
Hitachi ULSI Engineering Corp.	Tokyo			JP	03

APPL-NO: 09/ 551878 [PALM]
DATE FILED: April 18, 2000

PARENT-CASE:
This is a continuation application of U.S. Ser. No. 09/413,641, filed Oct. 6, 1999, now U.S. Pat. No. 6,097,663, which is a divisional application of U.S. Ser. No. 09/188,367, filed on Nov. 10, 1998, now U.S. Pat. No. 5,995,439, which is a continuation application of U.S. Ser. No. 08/813,900, filed on Mar. 7, 1997, now U.S. Pat. No. 6,069,834.

FOREIGN-APPL-PRIORITY-DATA:

COUNTRY	APPL-NO	APPL-DATE
JP	8-051321	March 8, 1996
JP	8-051330	March 8, 1996
JP	8-147010	June 10, 1996
JP	8-301538	November 13, 1996

INT-CL: [07] G11 C 8/00

US-CL-ISSUED: 365/230.03; 365/63, 365/189.08
US-CL-CURRENT: 365/230.03; 257/E27.097, 365/189.08, 365/63

FIELD-OF-SEARCH: 365/63, 365/52, 365/51, 365/230.03, 365/195, 365/189.08, 365/230.06

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PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected | Search ALL | Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	5371896	December 1994	Gove et al.	395/800
☐	5384745	January 1995	Konishi et al.	365/230.03
☐	5386391	January 1995	Watanabe	365/233
☐	5535161	July 1996	Kato	365/200
☐	5535172	July 1996	Reddy et al.	365/230.03
☐	5566371	October 1996	Ogawa	365/230.03
☐	5570319	October 1996	Santoro et al.	365/230.03
☐	5657273	August 1997	Ayukawa et al.	365/189.01
☐	5675537	October 1997	Bill et al.	365/185.22
☐	5691955	November 1997	Yamauchi	365/233
☐	5708612	January 1998	Abe	365/200
☐	5835424	November 1998	Kikukawa et al.	365/200
☐	5926431	July 1999	Toda	365/230.03
☐	5953278	September 1999	McAdams et al.	365/219
☐	5953280	September 1999	Matsui	365/230.03

FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
726 575	August 1996	EP	

OTHER PUBLICATIONS

IEEE Journal of Solid-State Circuit, vol. 30, No. 9, Sep. 1995, pp. 1006-1014.

ART-UNIT: 284

PRIMARY-EXAMINER: Elms; Richard

ASSISTANT-EXAMINER: Nguyen; Hien

ATTY-AGENT-FIRM: Mattingly, Stanger & Malur, P.C.

ABSTRACT:

A semiconductor IC device is designed using a memory core with a plurality of I/O lines, a transfer circuit module and a logic library which are produced beforehand and stored in a data base. The memory core and a logic circuit are arranged so that

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their I/O lines extend in the same direction. A transfer circuit including plural stages of switch groups is arranged between the I/O lines of the memory core and the I/O lines of the logic circuit. Switches forming each stage of switch group are formed between the I/O lines of the memory core and the I/O lines of the logic circuit. When one stage of or a small number of stages of switch groups are turned on, the I/O lines of the memory core and the I/O lines of the logic circuit are turned on, thereby forming a desired transfer pattern. The memory core is constructed by the combination of functional modules such as an amplifier module, a bank module and a power supply module. In the bank module are arranged row-system circuits which operate independently of each other and a multiplicity of I/O lines which extend in a bit line direction.

15 Claims, 85 Drawing figures

L5: Entry 1 of 43 File: USPT Aug 19, 2003

DOCUMENT-IDENTIFIER: US 6609236 B2
TITLE: Semiconductor IC device having a memory and a logic circuit implemented with a single chip

Brief Summary Text (14):
On the other hand, the second prior art concerns a coupling circuit for coupling memories and processors. In this second prior art, data transfer paths between the individual memories and the processors can be changed over to each other in various ways by crossbar switches. According to the second prior art, however, since the crossbar switches are used, a subject based on the above-mentioned second subject is caused. Namely, the second prior art has a subject that as the number of coupling lines is increased, the number of switches becomes enormous with an increase in scale of hardware and also an increase in delay. In the case where the data transfer paths between plural memories and plural processors independent of each other are changed over, as in the second prior art, a system used in the conventional parallel computer can be realized on the same chip, as it is, since the number of memories and processors is generally small. However, in the case where the correspondence between a group of several-hundred or more I/O lines of a memory and a group of I/O lines of a logic circuit such as operation circuit is changed over, the requirements for the degree of integration and the operating speed are severe and it is therefore difficult to use the conventional system, as it is.

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L5: Entry 1 of 43 File: USPT Aug 19, 2003

US-PAT-NO: 6609236
DOCUMENT-IDENTIFIER: US 6609236 B2

TITLE: Semiconductor IC device having a memory and a logic circuit implemented with a single chip

DATE-ISSUED: August 19, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Watanabe; Takao	Fuchu			JP
Ayukawa; Kazushige	Kokubunji			JP
Fujita; Ryo	Hitachi			JP
Yanagisawa; Kazumasa	Kokubunji			JP
Tanaka; Hitoshi	Ome			JP

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Hitachi, Ltd.	Tokyo			JP	03
Hitachi ULSI Systems Co., Ltd.	Tokyo			JP	03

APPL-NO: 09/ 964615 [PALM]
DATE FILED: September 28, 2001

PARENT-CASE:
This application is a continuation application of U.S. Ser. No. 09/808,943, filed Mar. 16, 2001, now U.S. Pat No. 6,335,898, which is a continuation application of U.S. Ser. No. 09/551,878, filed Apr. 18, 2000, now U.S. Pat. No. 6,246,629, which is a continuation application of U.S. Ser. No. 09/413,641, filed on Oct. 6, 1999, now U.S. Pat. No. 6,097,663, which is a divisional application of U.S. Ser. No. 09/188,367, filed Nov. 10, 1998, now U.S. Pat. No. 5,995,439, which is a continuation application of U.S. Ser. No. 08/813,900, filed Mar. 7, 1997, now U.S. Pat. No. 6,069,834.

FOREIGN-APPL-PRIORITY-DATA:

COUNTRY	APPL-NO	APPL-DATE
JP	08-051321	March 8, 1996
JP	08-051330	March 8, 1996
JP	08-147010	June 10, 1996
JP	08-301538	November 13, 1996

INT-CL: [07] G06 F 9/45

US-CL-ISSUED: 716/8; 716/9, 716/10
US-CL-CURRENT: 716/8; 257/E27.097, 716/10, 716/9

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FIELD-OF-SEARCH: 716/8-11, 716/17, 714/728, 714/738, 365/189.08, 365/230.03, 365/230.06, 365/207

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected | Search ALL | Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	5371896	December 1994	Gove et al.	712/20
☐	5384745	January 1995	Konishi et al.	365/230.03
☐	5386391	January 1995	Watanabe	365/233
☐	5535161	July 1996	Kato	365/200
☐	5535172	July 1996	Reddy et al.	365/230.03
☐	5566371	October 1996	Ogawa	365/230.03
☐	5570319	October 1996	Santoro et al.	365/230.03
☐	5657273	August 1997	Ayukawa et al.	365/189.01
☐	5675537	October 1997	Bill et al.	365/185.22
☐	5691955	November 1997	Yamauchi	365/233
☐	5708612	January 1998	Abe	365/200
☐	5835424	November 1998	Kikukawa et al.	365/200
☐	5926431	July 1999	Toda	365/230.03
☐	5953278	September 1999	McAdams et al.	365/219
☐	5953280	September 1999	Matsui	365/230.03
☐	5995439	November 1999	Watanabe et al.	365/230.03
☐	6246629	June 2001	Watanabe et al.	365/230.03

FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
726 575	August 1996	EP	

OTHER PUBLICATIONS

IEEE Journal of Solid-State Circuit, vol. 30, No. 9, Sep. 1995, pp. 1006-1014.

ART-UNIT: 2825

PRIMARY-EXAMINER: Siek; Vuthe

ATTY-AGENT-FIRM: Mattingly, Stanger & Malur, P.C.

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ABSTRACT:

A semiconductor IC device is designed using a memory core with a plurality of I/O lines, a transfer circuit module and a logic library which are produced beforehand and stored in a data base. The memory core and a logic circuit are arranged so that their I/O lines extend in the same direction. A transfer circuit including plural stages of switch groups is arranged between the I/O lines of the memory core and the I/O lines of the logic circuit. Switches forming each stage of switch group are formed between the I/O lines of the memory core and the I/O lines of the logic circuit. When one stage of or a small number of stages of switch groups are turned on, the I/O lines of the memory core and the I/O lines of the logic circuit are turned on, thereby forming a desired transfer pattern. The memory core is constructed by the combination of functional modules such as an amplifier module, a bank module and a power supply module. In the bank module are arranged row-system circuits which operate independently of each other and a multiplicity of I/O lines which extend in a bit line direction.

10 Claims, 84 Drawing figures

L5: Entry 7 of 43 File: USPT May 30, 2000

DOCUMENT-IDENTIFIER: US 6070003 A
TITLE: System and method of memory access in apparatus having plural processors and plural memories

Detailed Description Text (7):
As shown in FIG. 1, there is a set of parallel processors 100-103 and a master processor 12 connected to a series of memories 10 via a cycle-rate local connection network switch matrix 20 called a crossbar switch. The crossbar switch, as will be shown, is operative on a cycle by cycle basis to interconnect the various processors with the various memories so that different combinations of distributed and shared memory arrangements can be achieved from time to time as necessary for the particular operation. Also, as will be shown, certain groups of processors can be operating in a distributed mode with respect to certain memories, while other processors concurrently can be operating in the shared mode with respect to each other and with respect to a particular memory.

Detailed Description Text (39):
Turning now to FIG. 15, the MIMD mode is shown such that processors 100-103 are connected through crossbar switch 20 to various memories. Typically, these connections would last through several cycles and thus, the processors each would be connected to the respective memories for a period of time. While this is not necessary, it would be the most typical operation in the MIMD mode. For any processor, or group of processors operating in the MIMD mode of FIG. 15, crossbar switch 20 can, on a cycle by cycle basis, be operated so that data from a particular memory element is immediately made available to any of the other processors so that the data can either be cycled through the other processors or operated on a one-time basis.

Detailed Description Text (47):
Transfer processor 11 shown in FIGS. 1 and 2 and in FIG. 57 transfers data between external memory and the various internal memory elements. Transfer processor 11 is designed to operate from packet requests such that any of the parallel processors or the master processor can ask transfer processor 11 to provide data for any particular pixel or a group of pixels or data, and the transfer processor will transfer the necessary data to or from external and internal memory without further processor intervention instructions. This then allows transfer processor 11 to work autonomously and to process data in and out of the system without monitoring by any of the processors. Transfer processor 11 is connected to all of the memories through switch matrix 20 and is arranged to contend with the various links for access to the memories. Transfer processor 11 for any particular link may be assigned the lowest priority and access a memory when another processor is not accessing that memory. The data that is being moved by the transfer processor is not only the data for processing pixels, but instruction streams for controlling the system. These instruction streams are loaded into the instruction memory via crossbar switch 20. Transfer processor 11 can be arranged with a combination of hardware and software to effect the purpose of data transfer.

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L5: Entry 7 of 43 File: USPT May 30, 2000

US-PAT-NO: 6070003
DOCUMENT-IDENTIFIER: US 6070003 A

TITLE: System and method of memory access in apparatus having plural processors and plural memories

DATE-ISSUED: May 30, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Gove; Robert J.	Plano	TX		
Balmer; Keith	Bedford			GB
Ing-Simmons; Nicholas Kerin	Bedford			GB
Guttag; Karl Marion	Missouri City	TX		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Texas Instruments Incorporated	Dallas	TX			02

APPL-NO: 08/ 264582 [PALM]
DATE FILED: June 22, 1994

PARENT-CASE:
This application is a Continuation of application Ser. No. 07/437,852, filed Nov. 17, 1989 abandoned.

INT-CL: [07] G06 F 13/16

US-CL-ISSUED: 395/312
US-CL-CURRENT: 710/317

FIELD-OF-SEARCH: 395/200, 395/800

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4365292	December 1982	Barnes et al.	395/800
☐	4553203	November 1985	Rau et al.	395/800
☐	4562535	December 1985	Vincent et al.	364/200

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☐	4633245	December 1986	Blout et al.	340/825.03
☐	4644496	February 1987	Andrews	364/900
☐	4747043	May 1988	Rodman	364/200
☐	4807184	February 1989	Shelor	364/900
☐	4811201	March 1989	Rau et al.	395/325
☐	4930102	May 1990	Jennings	395/800
☐	4965718	October 1990	George et al.	395/800
☐	4985832	January 1991	Grondalski	395/800
☐	5020059	May 1991	Gonin et al.	395/800
☐	5041971	August 1991	Carvey et al.	395/800
☐	5056000	October 1991	Chang	395/800
☐	5083267	January 1992	Rau et al.	395/375
☐	5133073	July 1992	Jackson et al.	395/800
☐	5142686	August 1992	Hecht et al.	395/800

FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
0 245 996	November 1987	EP	
WO 88/08167	October 1988	WO	

OTHER PUBLICATIONS

A. M. Despain, et al., "High Performance Prolog, The Multiplicative Effect of Several Levels of Implementation", IEEE, pp. 178-184, 1986.
"VITec Parallel C Compiler", by T. Butler, published by Visual Information Technologies, Inc. Plano TX, pp. 741-747.
"A Single Board image computer with 64 Parallel Processors", by Stephen Wilson, published in Electronic Imaging '87, International Electronic Imaging Exposition & Conference, (1987) pp. 470-475.
"The Androx Parallel Image Array Processor", by Wayne Threatt, in Electronic Imaging '87, International Electronic Imagining Exposition & Conference (1987), pp. 1061-1064.
"Real Time 3D Object Tracking in a Rapid Prototyping Environment", by Robert J. Gove in Electronic Imaging '88 (1988).
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"The Use of Parallel-Processing Computers in Digital Image Processing", by Lew Brown, published by Alliant Computer Systems Corp., Litteton, MA.
"The Connection Machine", by W.D. Hillis, published in The MIT Press (1985).
"Handling Real Time Images Comes Naturally to Systolic Array Chip", by Hannaway, Shea Bishop, in Electronic Design, p. 289-300 (1984).
"Systolic Array Chip Recognizes Visual Patterns Quicker Than a Wink", by W.W. Smith, P. Sullivan, in Electronic Design, pp. 257-266 (1984).
"Design of a Massively Parallel Processor", by Kenneth Batcher, IEEE Transactions on Computers, v. C-29, No. 9 (1980).
"High Resolution Frame Grabbing and Processing Through Parallel Architecture", by

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Daniel Crevier published by Coreco, Inc., Quebec, Canada.
Multiple Digital Signal Processor Environment for Intelligent Signal Processing by Gass et al., in Proceedings of the IEEE, v. 75, No. 9 (Sep. 1987) pp. 1246-125.
"Architecture and Design of the Mars Hardware Accelerator", Agra Wall, et. in 24.sup.th ACM/IEEE Design Automation Conference (1987), pp. 101-107.
"Digital Video & Image Processors", by O'Brien, Mather & Holland, published by Plessey Semiconductors (1989).
"An Architectureal Study, Design and Implementation of Digital Image Acquisition, Processing and Display Systems with Micro-Processor-Based Personal Computers and Charge-Coupled Device Imaging Technology", a dissertation by Robert J. Go SMU (1986).
"A Medium Grained Parallel Computer for Image Processing", by R.S. Cok, published by Digital Technology Center, Eastman Kodak Co., Rochester NY.

ART-UNIT: 273

PRIMARY-EXAMINER: Teska; Kevin J.

ASSISTANT-EXAMINER: Choi; Kyle J.

ATTY-AGENT-FIRM: Marshall, Jr.; Robert D. Brady, III; W. James Telecky, Jr.; Frederick J.

ABSTRACT:

There is disclosed a multi-processor system and method arranged, in one embodiment, as an image and graphics processor. The image processor is structured with several individual processors all having communication links to several memories. A crossbar switch serves to establish the processor memory links. The entire image processor, including the individual processors, the crossbar switch and the memories, is contained on a single silicon chip.

16 Claims, 64 Drawing figures

L5: Entry 14 of 43 File: USPT Jun 16, 1998

DOCUMENT-IDENTIFIER: US 5768609 A
TITLE: Reduced area of crossbar and method of operation

Detailed Description Text (7):
As shown in FIG. 1, there is a set of parallel processors 100-103 and a master processor 12 connected to a series of memories 10 via a cycle-rate local connection network switch matrix 20 called a crossbar switch. The crossbar switch, as will be shown, is operative on a cycle by cycle basis to interconnect the various processors with the various memories so that different combinations of distributed and shared memory arrangements can be achieved from time to time as necessary for the particular operation. Also, as will be shown, certain groups of processors can be operating in a distributed mode with respect to certain memories, while other processors concurrently can be operating in the shared mode with respect to each other and with respect to a particular memory.

Detailed Description Text (37):
Turning now to FIG. 15, the MIMD mode is shown such that processors 100-103 are connected through crossbar switch 20 to various memories. Typically, these connections would last through several cycles and thus, the processors each would be connected to the respective memories for a period of time. While this is not necessary, it would be the most typical operation in the MIMD mode. For any processor, or group of processors operating in the MIMD mode of FIG. 15, crossbar switch 20 can, on a cycle by cycle basis, be operated so that data from a particular memory element is immediately made available to any of the other processors so that the data can either be cycled through the other processors or operated on a one-time basis.

Detailed Description Text (45):
Transfer processor 11 shown in FIGS. 1 and 2 and in FIG. 57 transfers data between external memory and the various internal memory elements. Transfer processor 11 is designed to operate from packet requests such that any of the parallel processors or the master processor can ask transfer processor 11 to provide data for any particular pixel or a group of pixels or data, and the transfer processor will transfer the necessary data to or from external and internal memory without further processor intervention instructions. This then allows transfer processor 11 to work autonomously and to process data in and out of the system without monitoring by any of the processors. Transfer processor 11 is connected to all of the memories through switch matrix 20 and is arranged to contend with the various links for access to the memories. Transfer processor 11 for any particular link may be assigned the lowest priority and access a memory when another processor is not accessing that memory. The data that is being moved by the transfer processor is not only the data for processing pixels, but instruction streams for controlling the system. These instruction streams are loaded into the instruction memory via crossbar switch 20. Transfer processor 11 can be arranged with a combination of hardware and software to effect the purpose of data transfer.

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L5: Entry 14 of 43 File: USPT Jun 16, 1998

US-PAT-NO: 5768609
DOCUMENT-IDENTIFIER: US 5768609 A

TITLE: Reduced area of crossbar and method of operation

DATE-ISSUED: June 16, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Gove; Robert J.	Plano	TX		
Balmer; Keith	Bedford			GB2
Ing-Simmons; Nicholas Kerin	Bedford			GB2
Guttag; Karl Marion	Missouri City	TX		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Texas Instruments Incorporated	Dallas	TX			02

APPL-NO: 08/ 483657 [PALM]
DATE FILED: June 7, 1995

PARENT-CASE:
This application is: a continuation of U.S. patent application Ser. No. 08/264,582 filed Jun. 22, 1994; which is a continuation of U.S. patent application Ser. No. 07/437,852 filed Nov. 17, 1989, now abandoned.

INT-CL: [06] G06 F 15/173, G06 F 15/80

US-CL-ISSUED: 395/800.11
US-CL-CURRENT: 712/11

FIELD-OF-SEARCH: 395/325, 395/375, 395/800, 395/400

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4365292	December 1982	Barnes et al.	395/800
☐	4807184	February 1989	Shelov	395/200
☐	4989131	January 1991	Stone	395/800

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☐	5056000	October 1991	Chang	395/800
☐	5107420	April 1992	Kametani	395/650
☐	5247689	September 1993	Ehlert	395/800

ART-UNIT: 273

PRIMARY-EXAMINER: Teska; Kevin J.

ASSISTANT-EXAMINER: Mohamed; Ayni

ATTY-AGENT-FIRM: Marshall, Jr.; Robert D. Kesterson; James C. Donaldson; Richard L.

ABSTRACT:

There is disclosed a multi-processor system and method arranged, in one embodiment, as an image and graphics processor. The image processor is structured with several individual processors all having communication links to several memories. A crossbar switch serves to establish the processor memory links. The entire image processor, including the individual processors, the crossbar switch and the memories, is contained on a single silicon chip.

26 Claims, 64 Drawing figures

First Hit Fwd Refs

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L5: Entry 17 of 43 File: USPT May 13, 1997

DOCUMENT-IDENTIFIER: US 5630162 A
TITLE: Array processor dotted communication network based on H-DOTs

Brief Summary Text (124):
U.S. Pat. No. 4,985,832 of Grondalski, entitled "SIMD Array Processing System with Routing Networks Having a Plurality of Switching Stages to Transfer Messages Among Processors", is another example of SIMD Array Processing Systems having routing networks. They address small groups of PEs that communicate via memory sharing; a NEWS mesh providing for regular array processing; a mechanism whereby PEs can share a large broadcast communication task; and a random routing network comprised of some "butterfly" stages followed by a 16.times.16 crossbar switch; but this patent focuses on random routing including a crossbar switch chip and its fault tolerant aspects. While this patent focuses on a number of communication schemes, it does not describe any dotted mechanism.

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L5: Entry 39 of 43 File: USPT Jul 25, 1989

DOCUMENT-IDENTIFIER: US 4852083 A
TITLE: Digital crossbar switch

Detailed Description Text (28):
The crossbar switch can be used to switch data and address interconnections among multiple processors and memories in a reconfigurable architecture. This architecture combines groups of processors and memories to form larger processor elements which can be configured to perform parallel processing. These same processing elements can be reconfigured dynamically to support alternative networks or processing structures.

First Hit Fwd Refs

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L5: Entry 39 of 43 File: USPT Jul 25, 1989

US-PAT-NO: 4852083
DOCUMENT-IDENTIFIER: US 4852083 A

TITLE: Digital crossbar switch

DATE-ISSUED: July 25, 1989

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Niehaus; Jeffrey A.	Dallas	TX		
Fleck; Robert G.	Dallas	TX		
Li; Stephen	Garland	TX		
Strong; Bob D.	Garland	TX		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Texas Instruments Incorporated	Dallas	TX			02

APPL-NO: 07/ 065231 [PALM]
DATE FILED: June 22, 1987

INT-CL: [04] H04M 3/18

US-CL-ISSUED: 370/58; 370/85, 370/112, 340/825.03
US-CL-CURRENT: 370/381; 340/2.28, 340/2.71, 370/362

FIELD-OF-SEARCH: 370/58, 370/59, 370/60, 370/64, 370/85, 370/67, 370/94, 370/53, 370/112, 364/200, 340/825.04, 340/825.03

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4084236	April 1978	Chelberg et al.	364/200
☐	4099234	July 1978	Woods et al.	364/200
☐	4404556	September 1983	Messina et al.	370/59
☐	4475187	October 1984	Barabas	370/59

OTHER PUBLICATIONS

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"The GF 11 Superconductors", IEEE, 1985, Beetem et al., pp. 108-115.
Digest of Technical Papers, 1987, IEEE International Solid State Circuits Conference, pp. 276, 277 and 425, Chi-Yuan Chin et al.

ART-UNIT: 214

PRIMARY-EXAMINER: Paschall; M. H.

ATTY-AGENT-FIRM: FitzGerald; Thomas R. Heiting; Leo N. Sharp; Melvin

ABSTRACT:

A digital crossbar switch for switching data from an input/output data bus to an internal data bus and to the same or another input/output data bus which includes a plurality of multiplexer logic units, an m-bit internal data bus coupled to each of said multiplexer logic units where m is an integer, and a plurality of n-bit input/output data buses one connected to each of the multiplexer logic units were n is an integer. The switch further includes an m/n to 1 multiplexer, where m/n is an integer, in each multiplexer logic unit. The m/n to 1 multiplexer has an input control to the internal data bus and an output coupled to a corresponding one of the input/output data buses and is operative in response to a configuration control signal to switch a selected n-bits of data from the internal data bus to the corresponding input/output data bus. A memory storage for storing configuration control signals is coupled to the m/n to 1 multiplexer.

24 Claims, 3 Drawing figures

US-PAT-NO: 6219627

DOCUMENT-IDENTIFIER: US 6219627 B1

TITLE: Architecture of a chip having multiple processors and multiple memories

---------- KWIC ---------

Detailed Description Text - DETX (2):
FIG. 1 is a schematic diagram depicting a system 12. The system 12 can be any system that uses an integrated circuit, such as any electronic entertainment device, any industrial equipment, any mainframe computer, minicomputer, personal computer, or workstation. The system 12 contains an integrated circuit 18. The integrated circuit contains a chip 20. FIG. 1 depicts an architecture 21 of the chip 20, illustrating modularity according to the preferred embodiment of the present invention. The architecture 21 contains several groups of processors 22 and memories 24, but only three such groups, 30, 32, and 34, of processors 22 and memories 24, are shown. The architecture 21 is built according to the invention earlier cross-referenced. Therefore, each processor 22 has direct communication with each memory 24, via a crossbar link 26, labeled "X-BAR". The box labeled "MASTER" is a master processor 27 to control the remaining co-processing elements. The box labeled "MOD-1" is a frame controller 28. However, MOD-1 can be any processing element. The frame controller 28 controls display units, such as CRT's and LCD's. The box labeled transfer processor is a transfer/memory processor 29, by which the processors 22 and 27 communicate with external devices, such as other memory, input/output devices, etc.

Detailed Description Text - DETX (6):
For example, if the architecture 21 is sliced at a point 50, the resulting integrated circuit 18 will contain the group 30, which contains one processor 22 and two memories 24. The processor 22 in the group 30 will communicate with the two memories 24 via the portion of the crossbar link 26 remaining in the group 30.

Detailed Description Text - DETX (11):

US006219627B1

(12) **United States Patent**
Bonneau et al.

(10) **Patent No.: US 6,219,627 B1**
(45) **Date of Patent: Apr. 17, 2001**

(54) **ARCHITECTURE OF A CHIP HAVING MULTIPLE PROCESSORS AND MULTIPLE MEMORIES**

(75) Inventors: **Walt C. Bonneau; Karl Guttag**, both of Missouri City; **Robert Gove**, Dallas, all of TX (US)

(73) Assignee: **Texas Instruments Incorporated**, Dallas, TX (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **08/274,132**

(22) Filed: **Jul. 12, 1994**

Related U.S. Application Data

(63) Continuation of application No. 07/813,857, filed on Dec. 26, 1991, now abandoned.

(51) **Int. Cl.**[7] **G06F 17/50**
(52) **U.S. Cl.** **703/1; 29/827**
(58) **Field of Search** 364/488–491; 347/51; 395/800; 703/1; 29/827

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,398,248	*	8/1983	Hsia et al.	395/425
4,491,907	*	1/1985	Koepper et al.	395/800
4,750,113	*	6/1988	Buggert	395/275
4,807,184	*	2/1989	Shelor	364/900
4,951,221	*	8/1990	Corbett et al.	364/489
4,968,977	*	11/1990	Chinnaswamy et al.	340/825.8
4,978,633	*	12/1990	Seefeldt	437/51
5,144,563	*	9/1992	Date et al.	364/491
5,175,824	*	12/1992	Soderbery et al.	395/325
5,200,908	*	4/1993	Date et al.	364/491
5,206,815	*	4/1993	Purcell	364/491
5,226,125	*	7/1993	Balmer et al.	395/325
5,280,620	*	1/1994	Sluijter et al.	395/800
5,345,228	*	9/1994	Franaszek et al.	340/825.79

OTHER PUBLICATIONS

Patent application entitled "Multi-processor With Crossbar Link of Processors and Memories, and Method of Operation", ser. no. 07/435,591, by Gove et al., filed Nov. 17, 1989, attorney docket number TI-14608.

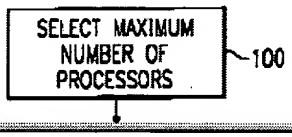
* cited by examiner

Primary Examiner—Zarni Maung
(74) *Attorney, Agent, or Firm*—Robert D. Marshall, Jr.; W. James Brady, III; Frederick J. Telecky, Jr.

(57) **ABSTRACT**

A method of manufacturing integrated circuits uses an architecture having multiple processors and multiple memories, such that there is at least first and second groups of processors and memories. The first group has at least a first processor and at least a first memory. The second group has at least a second processor and at least a second memory. Regardless of where the architecture is sliced, the integrated circuits have a majority of the same address and data pin-outs.

15 Claims, 5 Drawing Sheets



US-PAT-NO: 6262594

DOCUMENT-IDENTIFIER: US 6262594 B1

TITLE: Apparatus and method for configurable use of groups of pads of a system on chip

---------- KWIC ---------

Brief Summary Text - BSTX (5):

U.S. Pat. No. 5,701,507 describes an integrated circuit having several groups of processors and memories, wherein "each processor . . . has direct communication with each memory . . . via a crossbar link . . . " (column 3, lines 1-11). Moreover, U.S. Pat. No. 5,742,180 (see FIG. 1B) describes a gate array, wherein "nine (3.times.3) subarrays are connected by associated bidirectional cross bars . . . [c]communication at the edge of the nine subarrays goes off-chip via input/output pads or pins . . . " (column 6, lines 28-31).

First Hit Fwd Refs

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L3: Entry 1 of 1 File: USPT May 30, 2000

DOCUMENT-IDENTIFIER: US 6070003 A
TITLE: System and method of memory access in apparatus having plural processors and plural memories

Detailed Description Text (49):
The master processor, shown in more detail in FIG. 29, is used for scheduling and control of the entire system, including the control of the transfer processor as well as the interaction between the various processors. The master processor has a connection through the crossbar switch to all of the memories and is interconnected with the other processors on the communication channel. The master processor can control the type of data and the manner in which the data is obtained by the transfer processor depending upon the pixel information and the particular purpose for which the information is being obtained. Thus, regions of the image can be scanned under different scan modes depending upon the purpose for the scan. This is controlled by the master processor working in conjunction with the parallel processors. The parallel processors may each also control the transfer processor, either alone or in conjunction with the master processor, again depending upon the purpose for the operation.

Detailed Description Text (132):
The PC can be used to create instant data bases since the information put into the system can be read and the informational content abstracted immediately without further processing by other systems. This creates a data base that can be accessed simply by a match of particular words, none of which had been identified prior to the storage. This can be extended beyond words to geometric shapes, pictures and can be useful in many applications. For example, a system could be designed to scan a catalog, or a newspaper, to find a particular object, such as all of the trees or all of the red cars or all trucks over a certain size on a highway. Conceptually then, a data base would be formed by words, objects, and shapes which the image processor would abstract and make useful to the user.

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Search Results - Record(s) 1 through 10 of 15 returned.

☐ 1. Document ID: US 6260088 B1

L3: Entry 1 of 15 File: USPT Jul 10, 2001

US-PAT-NO: 6260088
DOCUMENT-IDENTIFIER: US 6260088 B1
**** See image for Certificate of Correction ****

TITLE: Single integrated circuit embodying a risc processor and a digital signal processor

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWMC | Draw De

☐ 2. Document ID: US 6070003 A

L3: Entry 2 of 15 File: USPT May 30, 2000

US-PAT-NO: 6070003
DOCUMENT-IDENTIFIER: US 6070003 A

TITLE: System and method of memory access in apparatus having plural processors and plural memories

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWMC | Draw De

☐ 3. Document ID: US 5768609 A

L3: Entry 3 of 15 File: USPT Jun 16, 1998

US-PAT-NO: 5768609
DOCUMENT-IDENTIFIER: US 5768609 A

TITLE: Reduced area of crossbar and method of operation

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWMC | Draw De

☐ 4. Document ID: US 5696913 A

L3: Entry 4 of 15 File: USPT Dec 9, 1997

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US-PAT-NO: 5696913
DOCUMENT-IDENTIFIER: US 5696913 A

TITLE: Unique processor identifier in a multi-processing system having plural memories with a unified address space corresponding to each processor

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 5. Document ID: US 5630162 A

L3: Entry 5 of 15 File: USPT May 13, 1997

US-PAT-NO: 5630162
DOCUMENT-IDENTIFIER: US 5630162 A

TITLE: Array processor dotted communication network based on H-DOTs

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 6. Document ID: US 5613146 A

L3: Entry 6 of 15 File: USPT Mar 18, 1997

US-PAT-NO: 5613146
DOCUMENT-IDENTIFIER: US 5613146 A

TITLE: Reconfigurable SIMD/MIMD processor using switch matrix to allow access to a parameter memory by any of the plurality of processors

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 7. Document ID: US 5522083 A

L3: Entry 7 of 15 File: USPT May 28, 1996

US-PAT-NO: 5522083
DOCUMENT-IDENTIFIER: US 5522083 A

TITLE: Reconfigurable multi-processor operating in SIMD mode with one processor fetching instructions for use by remaining processors

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 8. Document ID: US 5475856 A

L3: Entry 8 of 15 File: USPT Dec 12, 1995

US-PAT-NO: 5475856
DOCUMENT-IDENTIFIER: US 5475856 A

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TITLE: Dynamic multi-mode parallel processing array

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 9. Document ID: US 5471592 A

L3: Entry 9 of 15 File: USPT Nov 28, 1995

US-PAT-NO: 5471592
DOCUMENT-IDENTIFIER: US 5471592 A

TITLE: Multi-processor with crossbar link of processors and memories and method of operation

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 10. Document ID: US 5371896 A

L3: Entry 10 of 15 File: USPT Dec 6, 1994

US-PAT-NO: 5371896
DOCUMENT-IDENTIFIER: US 5371896 A

TITLE: Multi-processor having control over synchronization of processors in mind mode and method of operation

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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Terms	Documents
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L3: Entry 12 of 15 File: USPT Jul 6, 1993

US-PAT-NO: 5226125
DOCUMENT-IDENTIFIER: US 5226125 A

TITLE: Switch matrix having integrated crosspoint logic and method of operation

DATE-ISSUED: July 6, 1993

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Balmer; Keith	Bedford (Bedfordshire)			GB2
Ing-Simmons; Nicholas K.	Bedford (Bedfordshire)			GB2
Guttag; Karl M.	Missouri City (Harris County)	TX	77459	
Gove; Robert J.	Plano (Collin County)	TX	75075	

APPL-NO: 07/ 437875 [PALM]
DATE FILED: November 17, 1989

INT-CL: [05] G06F 13/14

US-CL-ISSUED: 395/325; 395/200, 340/825.79
US-CL-CURRENT: 710/317; 340/2.28

FIELD-OF-SEARCH: 364/DIG.1, 364/DIG.2, 340/825.79, 340/825.5, 340/825.51, 370/62, 370/58.3, 370/58.1, 395/200, 395/325

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	3581286	May 1971	Beausoleil	364/200
☐	3651473	March 1972	Faber	364/200
☐	3787818	January 1974	Arnold et al.	364/200
☐	4058316	November 1977	Miller	364/900
☐	4195344	March 1980	Yamazaki	364/200
☐	4562535	December 1985	Vincent et al.	364/200
☐	4644496	February 1987	Andrews	364/900
☐	4731724	March 1988	Mienzel et al.	364/200
☐	4747043	May 1988	Rodman	364/200

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☐	4905141	February 1990	Berenza	364/200
☐	4949280	August 1990	Littlefield	364/518
☐	4989131	January 1991	Stone	364/200
☐	5041971	August 1991	Carvey et al.	

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"A Single Board Image Computer with 64 Parallel Processes", by Stephen Wilson, published in Electronic Imaging '87, International Electronic Imaging Exposition & Conference, (1987), pp. 470-745.
"The Androx Parallel Image Array Processor", by Wayne Threatt, in Electronic Imaging '87, International Electronic Imaging Exposition & Conference, (1987), pp. 1061-1064.
"Design of a Massively Parallel Processor", by Kenneth Batcher, IEEE Transactions on Computers, vol. C-29, No. 9, (1980).
"High Resolution Frame Grabbing and Processing Through Parallel Architecture", by Daniel Crevier published by Coreco, Inc., Quebec, Canada.
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"Architecture and Design of the MARS Hardware Accelerator", Agra Wall et al., in 24th ACM/IEEE Design Automation Conference, (1987), pp. 101-107.
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"An Architecture Study, Design and Implementation of Digital Image Acquisition, Processing and Display Systems with Micro-Processor-Based Personal Computers and Charge-Coupled Device Imaging Technology", a dissertation by Robert J. Gove, S.M.U., (1986).
"A Medium Grained Parallel Computer for Image Processing", by R. S. Cok, published by Digital Technology Center, Eastman Kodak Co., Rochester, N.Y.

ART-UNIT: 237

PRIMARY-EXAMINER: Richardson; Robert L.

ATTY-AGENT-FIRM: Marshall, Jr.; Robert D. Kesterson; James C. Donalddson; Richard L.

ABSTRACT:

There is disclosed a switch matrix and operational method relying upon a high

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degree of operational logic at each matrix crosspoint. In one embodiment, the switch is used in a multiprocessor system arranged as an image and graphics processor. The processor is structured with several individual processors all having communication links to several memories without restriction. The switch matrix serves to establish the processor memory links and the entire image processor, including the individual processors, the crossbar switch and the memories and is contained on a single silicon substrate.

24 Claims, 64 Drawing figures